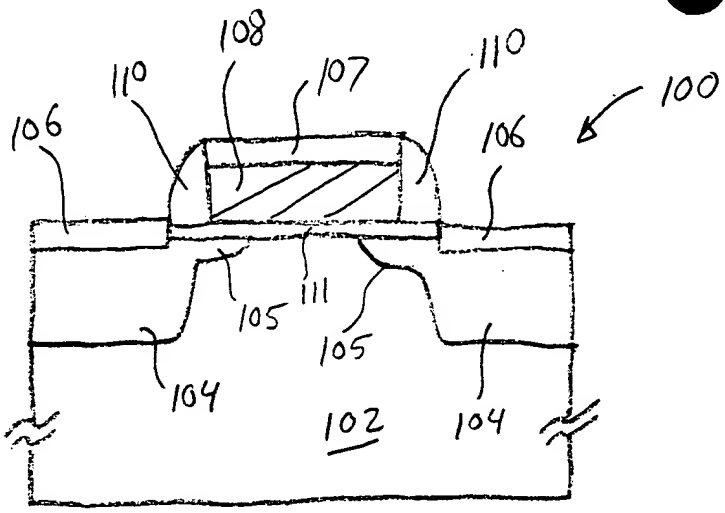

Fig. 1

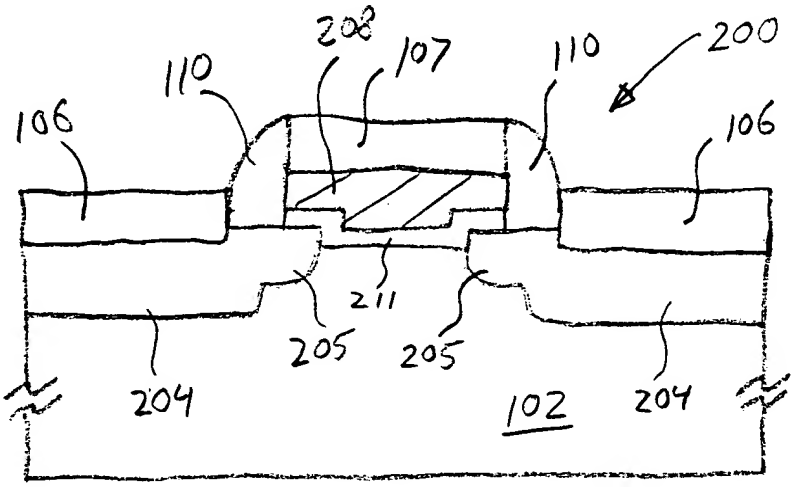

Fig. 2

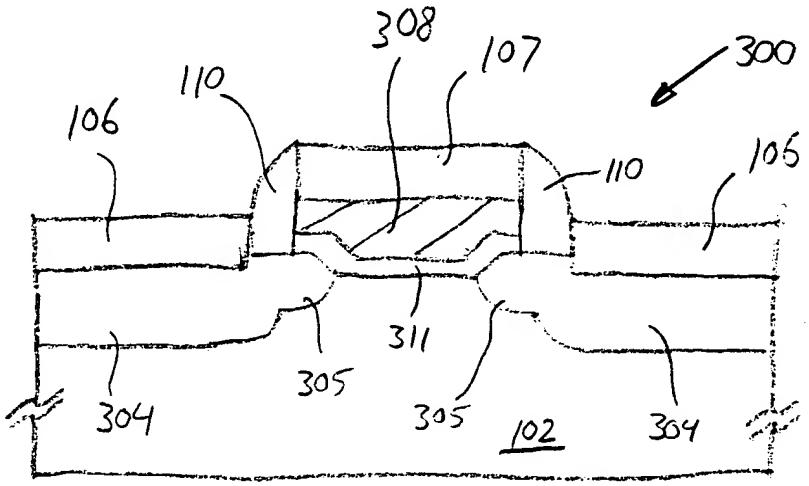

Fig. 3

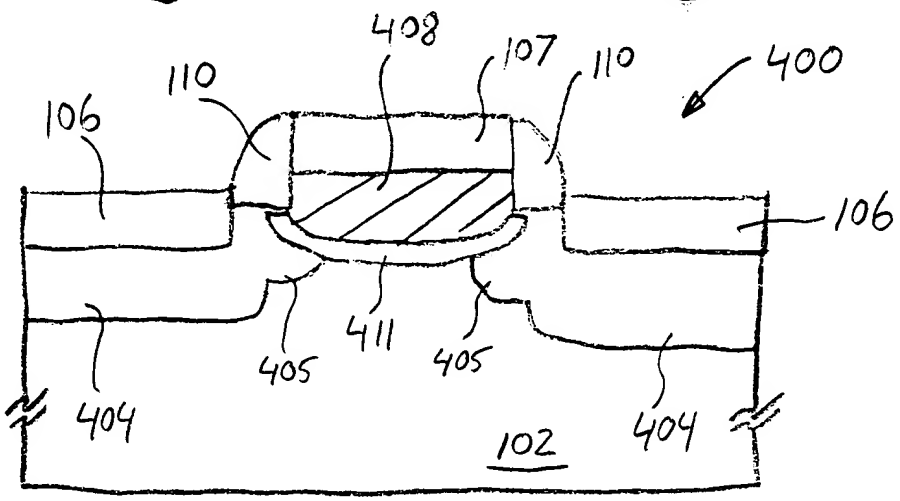

Fig. 4

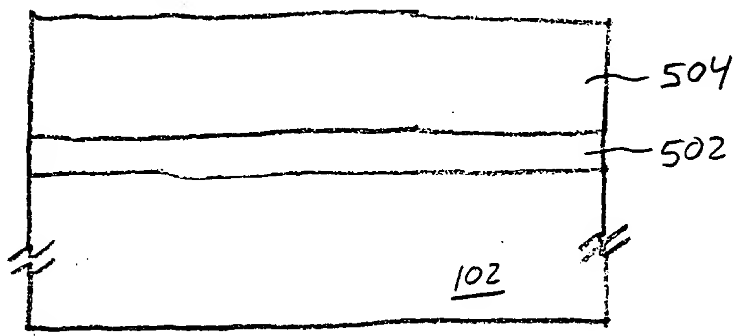

Fig. 5

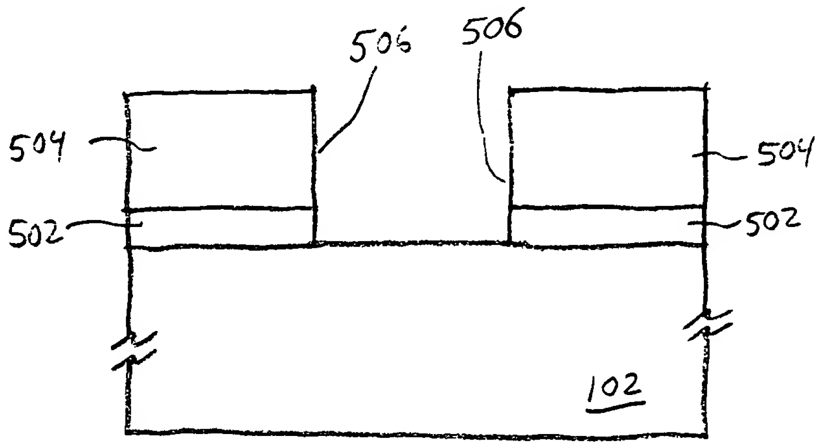

Fig. 6

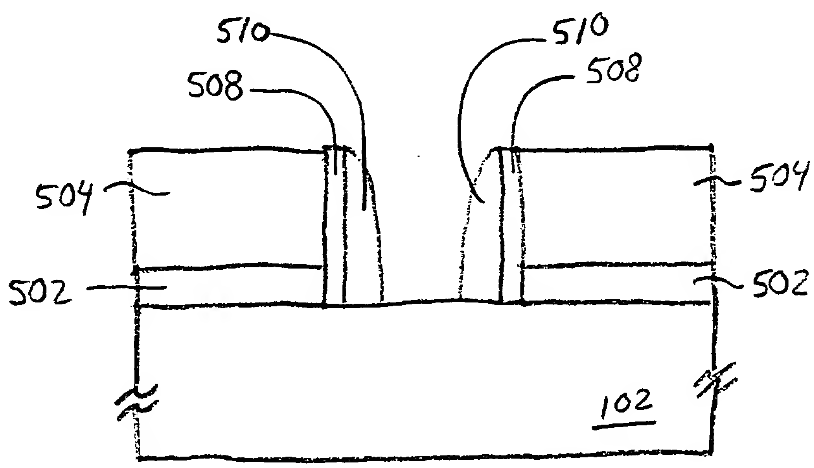

Fig. 7

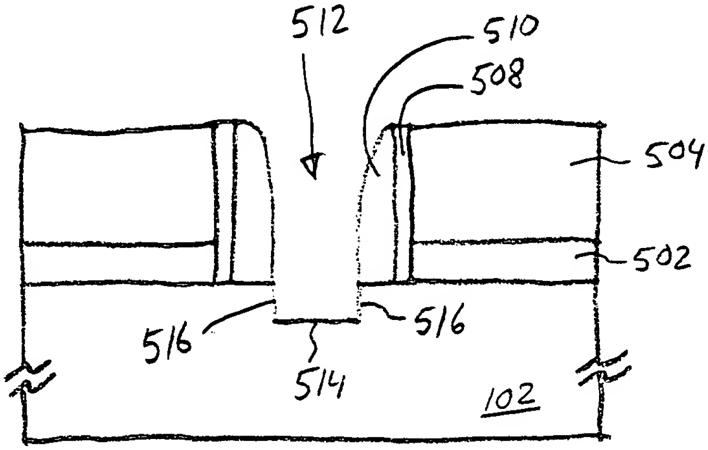

Fig. 8

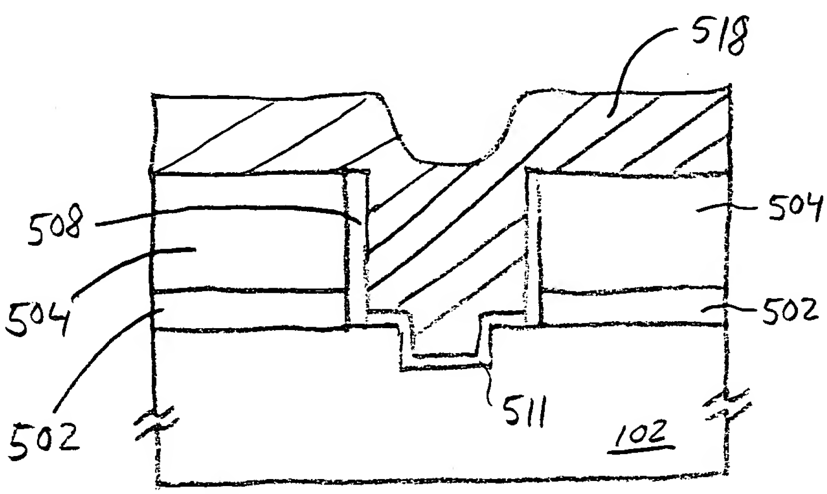

Fig. 9

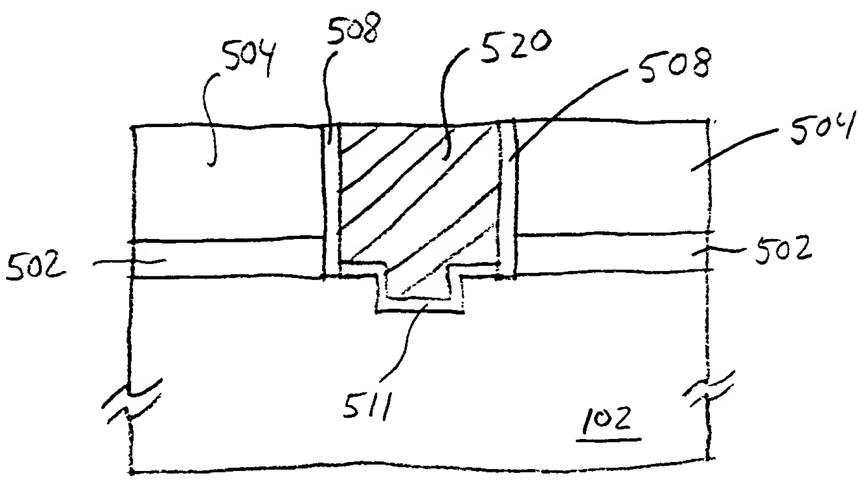

Fig. 10

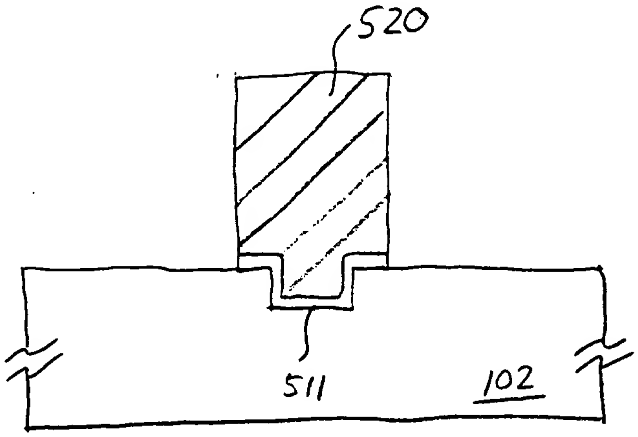

Fig. 11

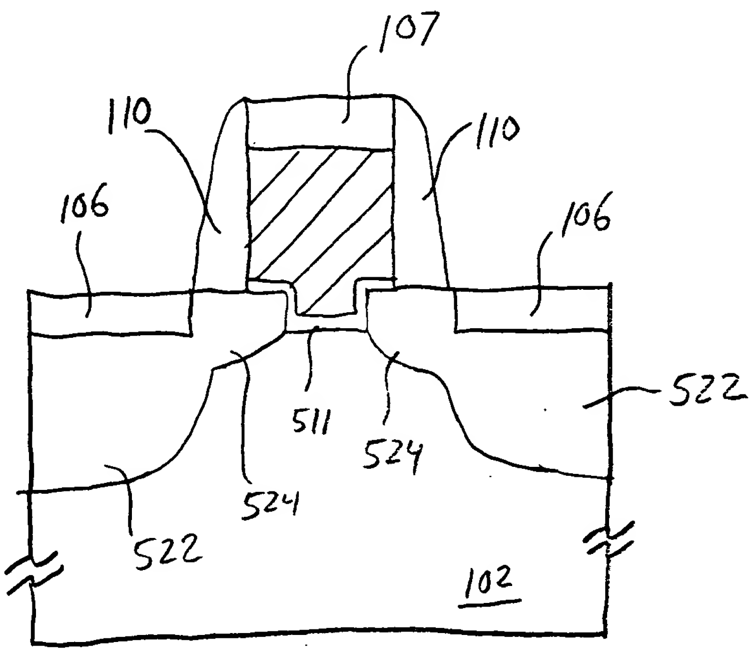

Fig. 12

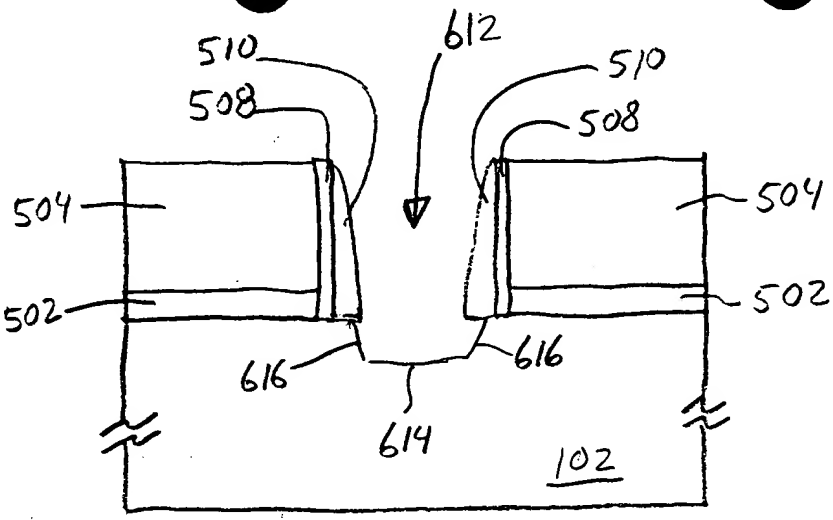
510
508
612
510
508
504
504
502
502
616
616
614
102

Fig. 13

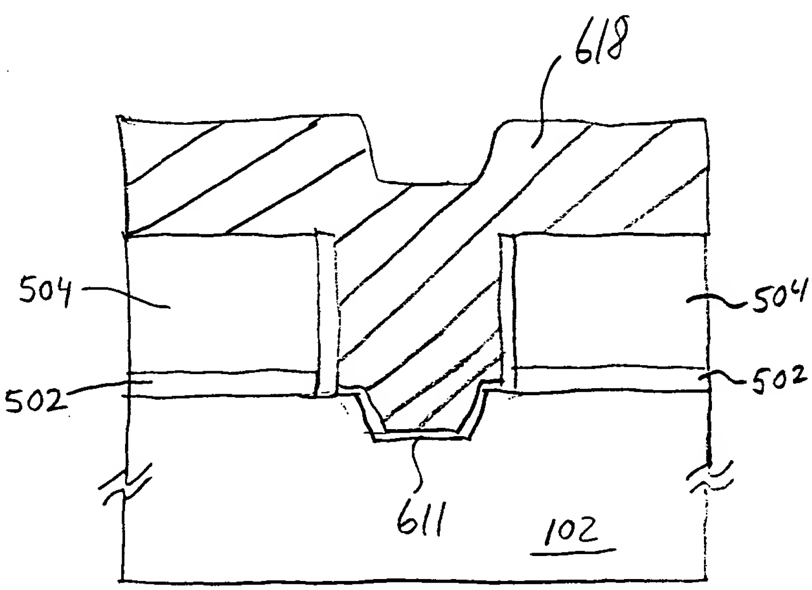
618
504
504
502
502
611
102

Fig. 14

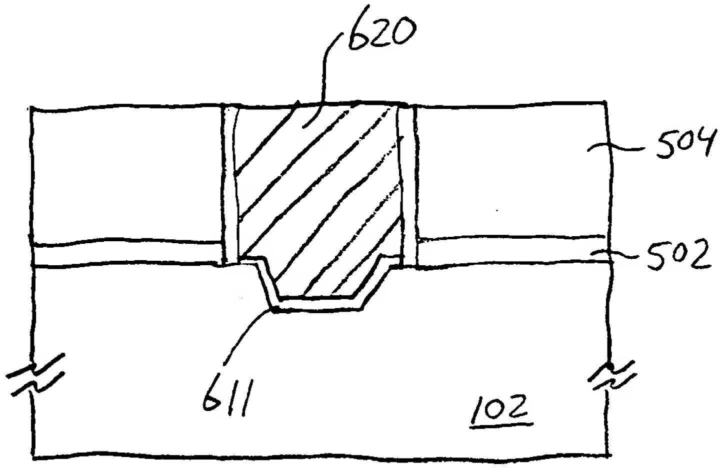

Fig. 15

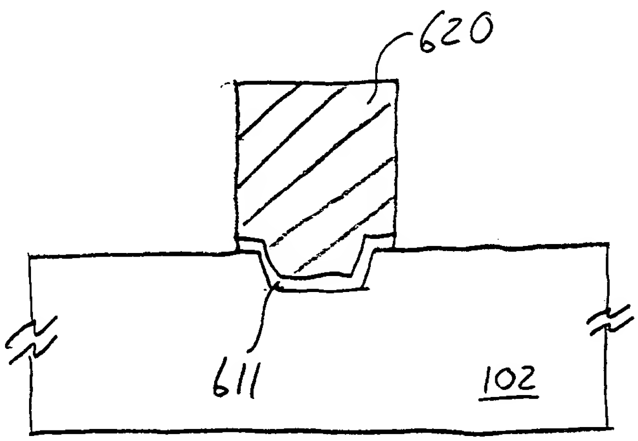

Fig. 16

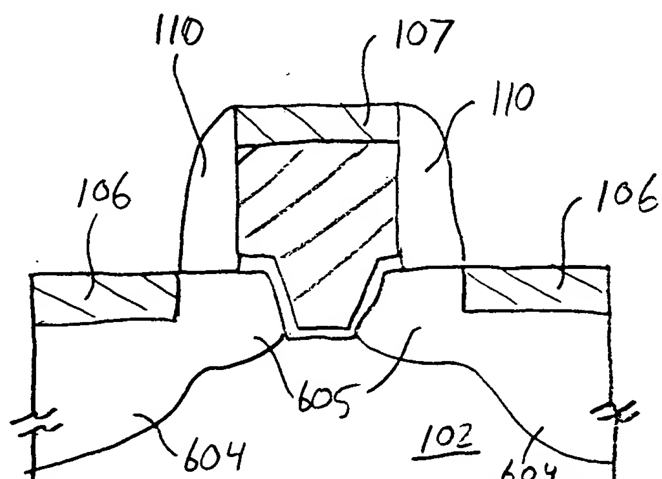

Fig. 17

P6892

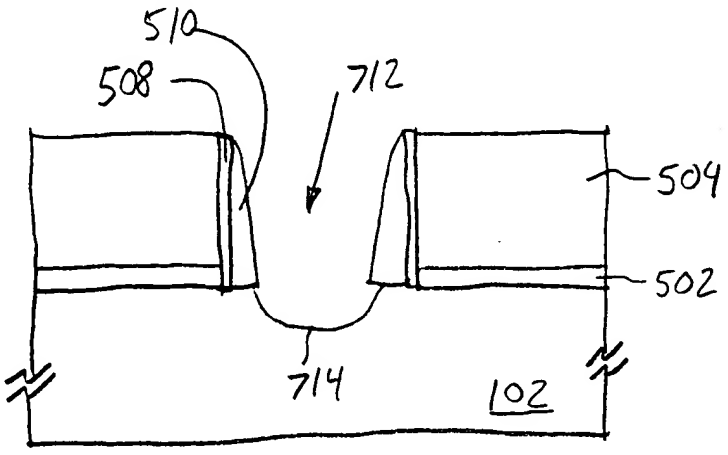

Fig. 18

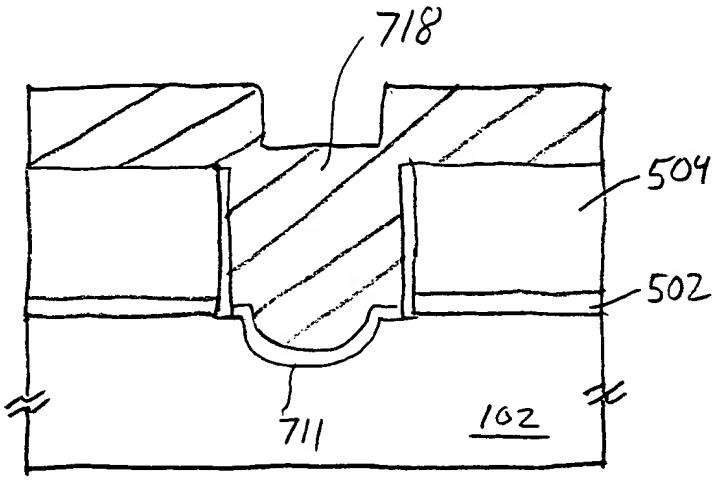

Fig. 19

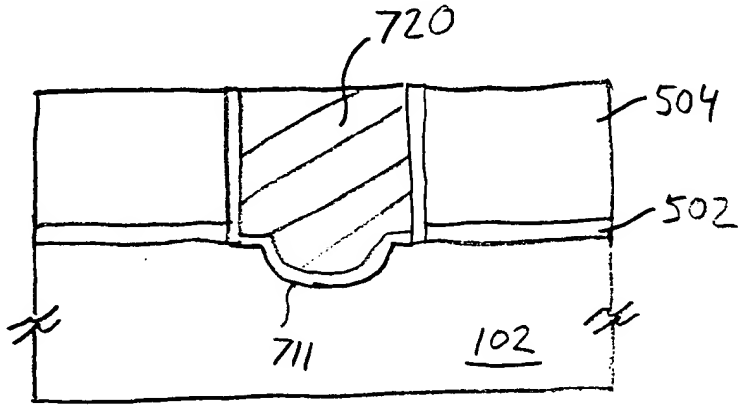

Fig. 20

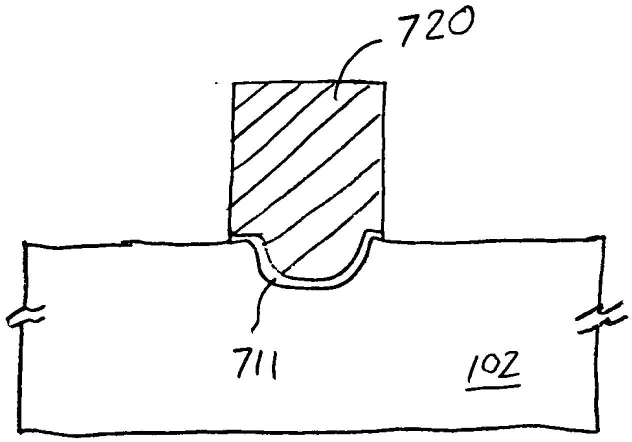

Fig. 21

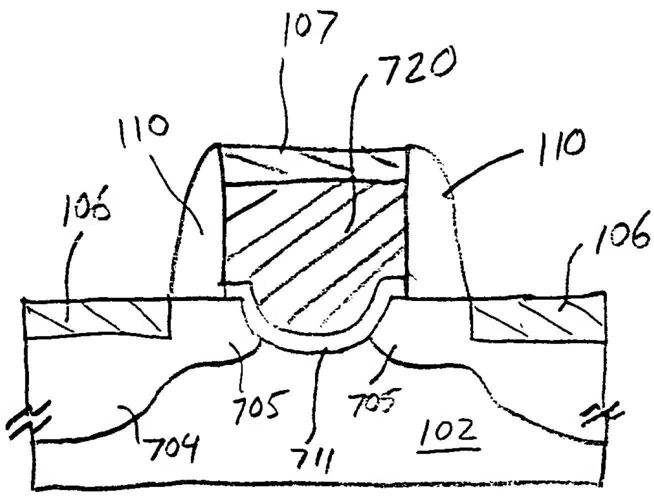

Fig. 22

2302

Pattern openings in a damascene layer on a wafer

2304

Form spacers along the sidewalls of the openings in the damascene layer

2306

Form recesses in the wafer at locations defined by the openings

2308

Form gate dielectric layer over at least the recesses

2310

Form gate electrode over the gate dielectric

2312

Form source/drain extension aligned with gate electrode

FIG. 23